REMARKS

Drawings

The Examiner has objected to Fig. 3b because the sectional portion of the drawing is not correctly referenced to Fig. 3d. Although the figures were not objected to in the original parent case, now U.S. Patent No. 6,016,390 ('390), a correction was made in the first divisional application, now U.S. Patent No. 6,470,304 ('304). The same correction that was made in the '304 case is made herein. Approval of the proposed change is respectfully requested.

Specification

The Examiner has stated that the "means for" language recited on page 7, line 7-10 of the specification is improper and does not provide the necessary enablement for the claimed subject matter. Applicant respectfully notes that the language the Examiner has objected to was allowed verbatim in the issued '390 and '304 patents. Although applicant believes the language proper, to expedite prosecution of this application, the "means for" language has been changed to "an automated circuit generator". The automated circuit generator is defined throughout the specification, which is used to generate the circuit designs. Removal of the objection is respectfully requested.

Claim Rejection- 35 USC Section 112, first paragraph

Applicant notes that the language the Examiner has cited as not complying with enablement requirements was allowed verbatim in the claims of both the '390 and '304 patents. As both issued patents are presumed valid, this language by definition has and does meet the enablement requirements of the code. The specification is quite clear that each separate wordline defines one additional word. Hence if there are 16 wordlines, the depth is 16. The specification also makes it clear that the exact number of words is irrelevant to the operation of the present invention. Similarly, each bitline pair defines a bit in the word. Thus, if there are 16 bitline pairs, the word width is 16. This is also clearly explained in the specification and also does not impact on the actual practice of the present invention.

Applicant believes this additional clarification should be sufficient to alleviate the Examiner's concern that the language is not enabling. Review and removal of this rejection is respectfully requested.

Claim Rejection- 35 U.S.C. 101- Same invention as U.S. Patent 6,016,390

Claims 1, 2, 5, 7, 8, 9, and 12 are amended herein. In particular, the six transistor limitation in claim 1 has been removed and the core cells have at least two bitlines and at least two complementary bitlines.

The claims in both the '304 and '390 were limited primarily to a core cell fabricated from six transistors. However, the teaching of the present invention clearly extends beyond this particular core cell to any core cell that is symmetrical about the axes as described within this application's specification and that uses bitline/bitline bar pairs to transmit the contents of the memory to and from the core cells. Multi-port core cells of various types meet this expanded definition and would not be covered by the claims of the '304 and '390 patents. As the scope of all the independent claims in this application as amended herein are broader than the issued independent claims in the '304 and '390 patents, the same invention is not being claimed in this application and the '390 patent. As different inventions are claimed, this rejection under 35 U.S.C. 101 for double patenting must be removed.

Claim Rejection- Obviousness-type Double Patenting

In response to this claim rejection, a Terminal Disclaimer is being filed with this response. The Disclaimer is a full response to the obviousness-type double patenting rejection.

Claim Rejection- 35 U.S.C. 103

Claims 1 through 14 are rejected under 35 U.S.C. 103 as unpatentable over the combination of Kornachuk et al., U.S. Patent 5,999,482 ('482) and Keeth, U. S. Patent No. 6,043,562 ('562).

Applicant is very aware of the teachings of the '482 patent, as he is one of the co-inventors of that patent. Although the core cells described therein are six transistor core cells, the depth of the memory is defined by the number of wordlines and the word width is defined by the number of bitline/bitline bar pairs, nothing in the '482 patent describes or even hints at the rotation of the core cell about its axes and coupling pairs of core cells and rotated (flipped) core cells to balance the bitline capacitances. The folding of the model wordlines in the '482 patent creates a self-timing path and in no way relates to the rotation of the core cells in the present application.

Despite the Examiner's assertions, nothing in the '562 patent supplies the teaching missing from the '482 reference. The core cells in the '562 are not rotated or flipped in any way. The Summary of the Invention makes clear that the digit line pairs are vertically twisted. The first and second digit lines are vertically offset. Although this is claimed to improve the signal-to-noise performance of the memory, it in no way resembles the rotation(flipping) of the core cells in the present invention.

Quite simply, neither reference describes or suggests constructing a memory from pairs of core cells and rotated (flipped) core cells. Without even a suggestion for such a construction in either reference, the combination cannot in any way make the present invention obvious.

A Notice of Allowance is therefore respectfully requested.

If the Examiner has any questions concerning the present amendment, the Examiner is kindly requested to contact the undersigned at (408) 749-6903. If any other fees are due in connection with filing this amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No ARTCP012B). A duplicate copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
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IN THE DRAWINGS

Amendment to the Drawings:

The attached sheet of drawings includes changes to Figure 3D.